

UD info Corp.

Industrial M.2 2242 PCIe SSD BM key M2P-42DP Series Product DataSheet



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Revision History

Revision	Draft Date	History	Author
1.0	2026/4/7	New release	Golden Lee



Product Overview

- **Capacity**
 - TLC: 256GB up to 2TB
 - pSLC: 80GB up to 640GB
- **Form Factor**
 - M.2 2242-S2-B-M
- **PCIe Interface**
 - PCIe Gen4 x2
 - NVMe 2.0
 - PCI Express Base 4.0
- **Flash Interface**
 - 256GB (80GB pSLC) = 256GB x 1pcs
 - 512GB (160GB pSLC) = 256GB x 2pcs
 - 1TB (320GB pSLC) = 512GB x 2pcs
 - 2TB (640GB pSLC) = 1024GB x 2pcs
- **Performance¹**
 - Seq. Read up to 3,500 MB/s
 - Seq. Write up to 3,300 MB/s
 - Ran. 4K Read up to 800K IOPS
 - Ran. 4K Write up to 750K IOPS
- **Power Consumption²**
 - Active mode (Max.): < 2.9W
 - Idle mode: < 0.9W
- **Reliability**
 - MTBF³: 4 million hours
 - UBER⁴: < 1 sector per 10¹⁶ bits
 - DWPD⁵:
 - TLC: ≥ 0.7
 - pSLC: ≥ 55
 - TBW⁵:
 - TLC: up to 2,690 TB
 - pSLC: up to 40,895 TB
- **Temperature Range⁶**
 - Operation Temperature:
 - Standard: 0°C ~ 70°C
- **ECC**
 - LDPC (Low Density Parity Check)
 - RAID ECC
- **Power Management (Optional, default not support)**
 - PS0/PS1/PS2/PS3/PS4
 - Support APST
 - Support ASPM
 - Support L1.2 (<5mW)
- **Environment Specification**
 - Shock:
 - 1000G_{0-P}/0.5ms duration (Operational)
 - 1500G_{0-P}/0.5m s duration (Non-operational)
 - Vibration:
 - 7Hz~800Hz/3.08Grms with random waveform (Operational)
 - 20Hz~80Hz/1.52mm 80Hz~2000Hz/20G_{P-P} with sine waveform (Non-operational)
 - Drop: 80cm height/each face
 - Conflicting Material: Concrete floor
- **RoHS Compliant**
- **EMI Compliant**
 - EN55032/55035, CISPR 32 (CE)
 - AS/NZS CISPR 32 (CE)
 - ANSI C63.4 (FCC)
- **Features Support List**
 - HMB (Host Memory Buffer)
 - TCG Pyrite/OPAL⁷
 - ETEDPP (End to End Data Path Protection)
 - Read Only Mode (End of Life)

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- Wide: -40°C ~ 85°C
- Storage Temperature: -40°C ~ 85°C

Notes:

1. For more details on Performance, please refer to Chapter 2.3.
2. For more details on Power Consumption, please refer to Chapter 4.2.
3. Mean Time Between Failure (MTBF)
4. Uncorrectable Bit Error Rate (UBER)
5. For more details on TBW/DWPD, please refer to Chapter 3.2.
6. The operation temperature means NAND case temperature, which mechanism is described in Chapter 2.5.
7. Supported by different production settings.

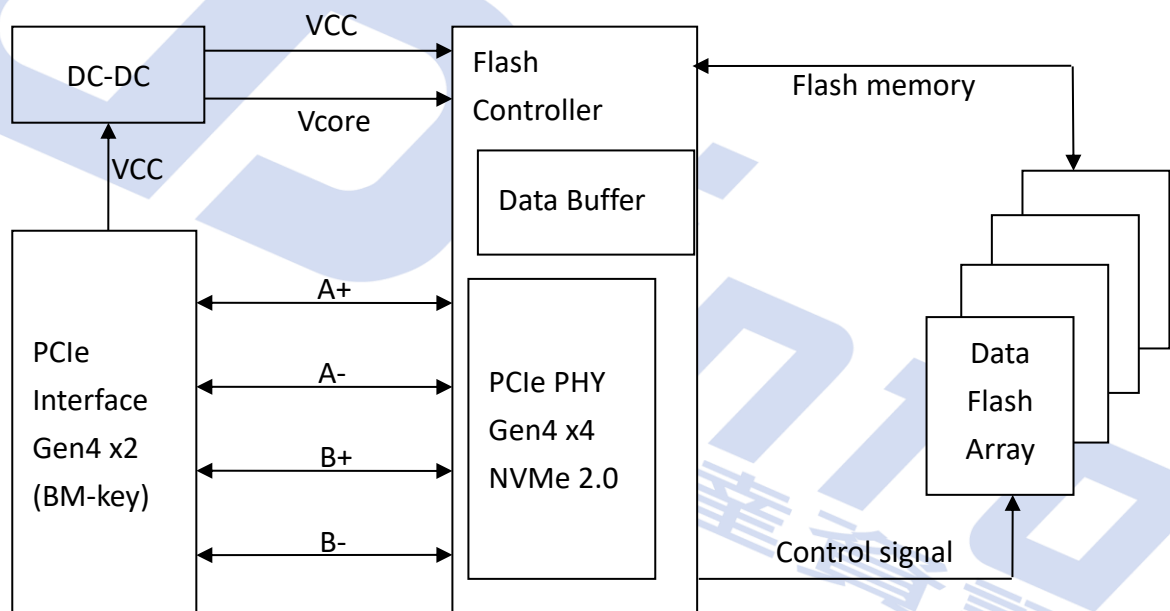


1. INTRODUCTION

1.1. General Description

UDinfo's M.2 2242 PCIe solid state Drive delivers all the advantages of flash disk technology with PCIe Gen4 x2 interface, including being fully compliant with the standard Next Generation Form Factor (NGFF) called M.2 form factor, providing low power consumption compared to traditional hard drive and hot-swapping when removing/replacing/upgrading flash disks. The device is designed based on the M.2 2242 standard. It offers up to 2TB and performance can reach up to 3,500MB/s read as well as 3,300MB/s write high performance based on 218Layers 3D TLC NAND flash.

1.2. Block Diagram



M.2 2242 PCIe SSD Block Diagram

2. PRODUCT SPECIFICATIONS

2.1. Product Specifications

- Capacity
 - TLC: 256GB up to 2TB
 - pSLC: 80GB up to 640GB
- Electrical/Physical Interface
 - PCIe Interface
 - PCI Express Base Ver 4.0
 - Compliant with NVMe 2.0
 - PCIe Gen4 x 2 lane & backward compatible to PCIe Gen3, Gen2 and Gen1
 - Support up to QD 128 with queue depth of up to 64K
 - PCI Express M.2 Specification Revision 4.0, Version 1.0

2.2. Device Capacity

Capacity	IDEMA Standard		User Data Size
	512Bytes/Sector	4KBytes/Sector	
	Total Sectors (LBA)	Total Sectors (LBA)	
256GB	500,118,192	62,514,774	Depended on file management
512GB	1,000,215,216	125,026,902	
1TB	2,000,409,264	250,051,158	
2TB	4,000,797,360	500,099,670	
80GB	156,301,488	19,537,686	
160GB	312,581,808	39,072,726	
320GB	625,142,448	78,142,806	
640GB	1,250,263,728	156,282,966	

Notes:

1. 1 Gigabyte (GB) is equal to 1,000,000,000 Bytes; 1 sector is equal to 512 Bytes or 4K Bytes.
2. The calculation is following IDEMA Standard.
3. The total actual user data size of the SSD may be less than device capacity due to SSD format, SSD partition, operating system.

EX: OS shows 476.94GB (NTFS) with 512GB SSD.

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2.3. Performance

- **Burst Sequential Read/Write Performance (MB/s)**

Capacity	Flash Structure	Sequential (MB/s) Standard-Temp.		Sequential (MB/s) Wide-Temp.	
		Read	Write	Read	Write
256GB	256GB x1, BGA(DDP), TLC	3,500	3,000		
512GB	256GB x2, BGA(DDP), TLC	3,500	3,200		
1TB	512GB x2, BGA(QDP), TLC	3,500	3,300		
2TB	1TB x2, BGA(ODP), TLC	3,500	3,300		
80GB	256GB x1, BGA(DDP), pSLC	3,500	3,000	3,500	3,000
160GB	256GB x2, BGA(DDP), pSLC	3,500	3,100	3,500	3,100
320GB	512GB x2, BGA(QDP), pSLC	3,500	3,200	3,500	3,200
640GB	1TB x2, BGA(ODP), pSLC	3,500	3,300	3,500	3,300

- **Sustained Sequential Read/Write Performance (MB/s)**

Capacity	Flash Structure	Sequential (MB/s) Standard-Temp.		Sequential (MB/s) Wide-Temp.	
		Read	Write	Read	Write
256GB	256GB x1, BGA(DDP), TLC	3,300	250		
512GB	256GB x2, BGA(DDP), TLC	3,300	500		
1TB	512GB x2, BGA(QDP), TLC	3,300	700		
2TB	1TB x2, BGA(ODP), TLC	3,300	1,200		
80GB	256GB x1, BGA(DDP), pSLC	3,300	3,000	3,300	3,000
160GB	256GB x2, BGA(DDP), pSLC	3,300	3,100	3,300	3,100
320GB	512GB x2, BGA(QDP), pSLC	3,300	3,200	3,300	3,200
640GB	1TB x2, BGA(ODP), pSLC	3,300	3,300	3,300	3,300

Notes:

1. Performance may differ according to flash configuration, use condition, environment and platform.
2. Performance specification is under that Thermal Throttling has not worked yet.
3. Performance is measured with the follow conditions
 - (a.) CrystalDiskMark 8.0.4 with QD8T1, 1GB range for Burst sequential.
 - (b.) Fio on Linux v5.10.32-ryder-20211006 with QD32T1, and SSD is fully written for Sustained sequential.
 - (c.) OS: Win11 64bit for Burst sequential.
 - (d.) OS: Ubuntu 20.04.2 LTS for Sustained sequential.

(e.) AMD Ryzen 7 7700X 8-Core Processor

4. Measurement environment: Room temperature: 20~25°C, humidity: 40~60%RH, DC+3.3V condition.

● **Burst Random Read/Write Performance (IOPS)**

Capacity	Flash Structure	Random (IOPS) Standard-Temp.		Random (IOPS) Wide-Temp.	
		Read	Write	Read	Write
256GB	256GB x1, BGA(DDP), TLC	360K	700K		
512GB	256GB x2, BGA(DDP), TLC	700K	750K		
1TB	512GB x2, BGA(QDP), TLC	800K	750K		
2TB	1TB x2, BGA(ODP), TLC	800K	750K		
80GB	256GB x1, BGA(DDP), pSLC	360K	700K	360K	700K
160GB	256GB x2, BGA(DDP), pSLC	700K	750K	700K	750K
320GB	512GB x2, BGA(QDP), pSLC	800K	750K	800K	750K
640GB	1TB x2, BGA(ODP), pSLC	800K	750K	800K	750K

● **Sustained Random Read/Write Performance (IOPS)**

Capacity	Flash Structure	Random (IOPS) Standard-Temp.		Random (IOPS) Wide-Temp.	
		Read	Write	Read	Write
256GB	256GB x1, BGA(DDP), TLC	85K	5K		
512GB	256GB x2, BGA(DDP), TLC	110K	8K		
1TB	512GB x2, BGA(QDP), TLC	120K	10K		
2TB	1TB x2, BGA(ODP), TLC	150K	11K		
80GB	256GB x1, BGA(DDP), pSLC	200K	21K	200K	21K
160GB	256GB x2, BGA(DDP), pSLC	300K	23K	300K	23K
320GB	512GB x2, BGA(QDP), pSLC	370K	25K	370K	25K
640GB	1TB x2, BGA(ODP), pSLC	360K	26K	350K	26K

Notes:

- Performance may differ according to flash configuration, use condition, environment and platform.
- Performance specification is under that Thermal Throttling has not worked yet.
- Performance is measured with the follow conditions
 - IOmeter v1.1.0 with QD32T16, 1GB range for 4KB Burst random.
 - Fio on Linux v5.10.32-ryder-20211006 with QD32T8, and SSD is fully written for 4KB Sustained random.
 - OS: Win11 64bit for Burst random.

- (i.) OS: Ubuntu 20.04.2 LTS for Sustained random.
 - (j.) AMD Ryzen 7 7700X 8-Core Processor
4. Measurement environment: Room temperature: 20~25°C, humidity: 40~60%RH, DC+3.3V condition.

2.4. POR/SPOR Standby Ready Time

- POR/SPOR Ready Time

Capacity	POR ready time		SPOR ready time	
	Typ.	Max.	Typ.	Max.
256GB (80GB pSLC)	100	300	2,000	10,000
512GB (160GB pSLC)	100	300	3,000	10,000
1TB (320GB pSLC)	100	300	3,000	10,000
2TB (640GB pSLC)	100	300	4,000	12,000

Unit: ms

Notes:

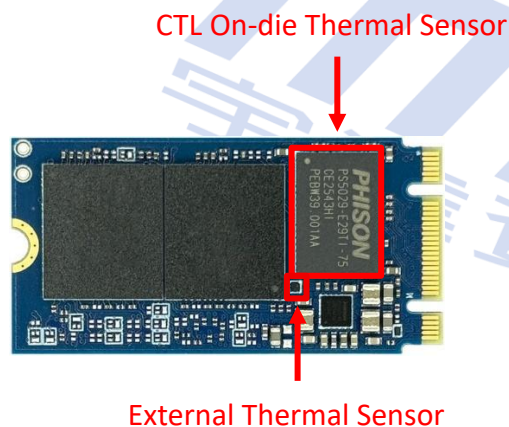
1. POR/SPOR stands for following:
 - (a.) POR: Power On Ready. (The ready time variation depends on data recover size.)
 - (b.) SPOR: Power On Ready after Sudden Power Off. (The ready time variation depends on data recover size.)
2. POR/SPOR ready time stands for following:

The time interval includes SSD power on and responses first I/O completed to host.
3. Measurement environment: Room temperature: 20~25°C, humidity: 40~60%RH, DC+3.3V condition.
4. These data will be affected by different platforms and conditions.

2.5. Thermal Throttling

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. The controller is designed with an on-die thermal sensor and with its accuracy, firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via S.M.A.R.T. reading.

- **Purpose of Thermal Throttling:**
 - In order to keep the optimal performance in the safe range of the temperature.
- **Thermal sensors:**
 - There are controller on-die sensor & external thermal sensor to detect SSD temperature.
(The thermal sensor is shown below. The picture is for reference only).
 - Controller on-die sensor detects controller temperature itself, while external thermal sensor helps to detect NAND temperature.
 - S.M.A.R.T. value shows the NAND temperature as Thermal Throttling triggered point.



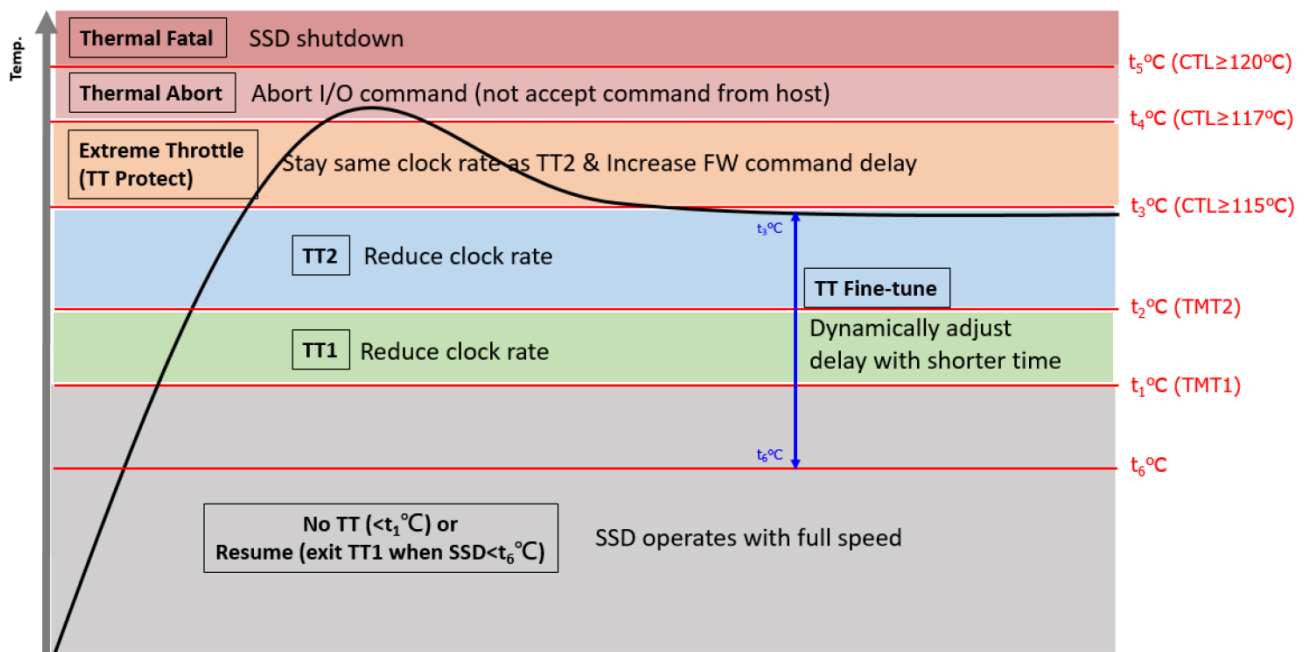


Figure 2-1 Thermal Throttling Schematic

	Stage	Status	Operation temp.
t ₁ /t ₆	No TT/Resume	SSD operates with full speed	<82°C / <74°C
t ₁	TT1	Reduce clock rate and increase firmware command delay	82°C
t ₂	TT2	Keep same clock rate as TT1, but increase more firmware command delay	85°C
t ₃ ~t ₆	TT Fine-tune	Dynamically adjust delay with shorter time	74°C ~ 95°C
t ₃	Extreme Throttle (TT Protect)	Reduce more clock rate and increase firmware command delay	95°C (or CTL ≥ 115°C)
t ₄	Thermal Abort	Abort I/O command (not accept I/O command from host)	98°C (or CTL ≥ 117°C)
t ₅	Thermal Fatal	SSD shutdown	100°C (or CTL ≥ 120°C)

Notes:

1. Operation temp. in Thermal Throttling Temperature Setting table means NAND temperature, which can be read by S.M.A.R.T.

2.6. TCG Opal 2.0 (Optional)

The Opal specification is a set of specifications for self-encrypting drives published by the Trusted Computing Group (TCG), a non-profit organization that develops, defines, and promotes standards and specifications for secure computing. The Opal Security Subsystem Class(SSC) 2.0 defines the details of data management in storage devices and the classes authority for data access, and secures data from theft and tampering by unauthorized persons who are able to gain access to the storage device or host system.

TCG Opal 2.0 Main Features:

- AES 256-bit Hardware Self Encryption
- Deploy Storage Device & Take Ownership:
The Storage Device is integrated into its target system and ownership transferred by setting or changing the Storage Device's owner credential.
- Activate or Enroll Storage Device:
LBA ranges are configured and data encryption and access control credentials (re)generated and/or set on the Storage Device. Access control is configured for LBA range unlocking.
- Lock & Unlock Storage Device:
Unlocking of one or more LBA ranges by the host and locking of those ranges under host control via either an explicit lock or implicit lock triggered by a reset event. MBR shadowing provides a mechanism to boot into a secure pre-boot authentication environment to handle device unlocking.
- Repurpose & End-of-Life:
Erasure of data within one or more.
- Physical Presence SID (PSID):
PSID is defined by TCG OPAL as a 32-character string and the purpose is to revert SSD back to its manufacturing setting when the drive is still OPAL-activated. PSID code can be printed on a SSD label when an OPAL-activated SSD supports PSID revert feature.

3. ENVIRONMENTAL SPECIFICATIONS



3.1. Environmental Conditions

3.1.1. Temperature Specification

	Mode	Min.	Max.	Unit
Temperature Ranges	Operation (Standard)	0	70	°C
	Operation (Wide)	-40	85	°C
	Storage	-40	85	°C
Humidity	Operation	5	95	%
	Storage	5	95	%
Temperature Cycle Test	Operation (Standard)	0	70	°C
	Operation (Wide)	-40	85	°C
	Storage	-40	85	°C

Notes:

The operation temperature means the case temperature. Airflow is suggested and it will allow device to be operated at appropriate temperature for each component during heavy workloads environment.

3.1.2. Mechanical Specification

Items			Condition
Shock	Operational	Acceleration Force	1000G 0-p with half sine wave (0.5ms)
	Non-operational	Acceleration Force	1500G 0-p with half sine wave (0.5ms)
Vibration	Operational	Frequency/Grms	7Hz~800Hz/3.08Grms with random waveform
	Non-operational	Frequency/Displacement	20Hz~80Hz/1.52mm p-p
		Frequency/Acceleration	80Hz~2000Hz/20G p-p with sine wave
Bending	Non-operational	≥ 20N	Hold 1min/5times
Drop	Non-operational	Height of Drop	80cm free fall
		Number of Drop	6 face of each unit
		Conflicting Material	Concrete floor

3.1.3. Electrostatic Discharge (ESD)

Specification	+/- 4KV
EN 55035, CISPR 35 EN 61000-4-2 and IEC 61000-4-2	Device functions are affected, but EUT will be back to its normal or operational state automatically.

3.1.4. EMI Compliance

Specification
EN 55032/55035, CISPR 32 (CE)
AS/NZS CISPR 32 (CE)
ANSI C63.4 (FCC)

3.1.5. Certification & Compliance

Specification
RoHS
WHQL
PCI Express Base 4.0
UNH-IOL NVM Express Logo

3.2. TBW (TeraBytes Written) and DWPD (Drive Write Per Day)

Capacity	Flash Type	TBW	DWPD
256GB	256GB x1, BGA(DDP), TLC	212	0.75
512GB	256GB x2, BGA(DDP), TLC	524	0.93
1TB	512GB x2, BGA(QDP), TLC	1,288	1.14
2TB	1TB x2, BGA(ODP), TLC	2,690	1.19
80GB	256GB x1, BGA(DDP), pSLC	4,895	55.87
160GB	256GB x2, BGA(DDP), pSLC	10,077	57.51
320GB	512GB x2, BGA(QDP), pSLC	20,258	57.81
640GB	1TB x2, BGA(ODP), pSLC	40,895	58.35

Notes:

- TBW is measured by JEDEC Client 219A workload.
 - TLC: Calculated with PE count = 3,000.
 - pSLC: Calculated with PE count = 100,000.
- TBW may differ according to flash configuration and platform configuration.
- DWPD is calculated based on 3-year lifetime.
- $DWPD = TBW / (365 \times 3\text{years} \times \text{User capacity})$
- The SSD supports trim function. If Operation System does not support trim command, performance and TBW will be affected. (Like certain Windows OS, Linux kernel version before 2.6.33, other OS please refer to respective user manual)

- The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor.

3.3. UBER

Capacity	UBER
TLC: 256GB ~ 2TB pSLC: 80GB ~ 640GB	< 1 sector per 10 ¹⁶ bits read

Notes:

- UBER (Uncorrectable Bit Error Rates) means the uncorrectable error per bits read.
- UBER = FER (fail rate) / Data Size (user data bit).
- FER = uncorrectable ECC frame number / total ECC frame number.
- The LDPC for TLC ECC capability > 120bit/KB.

3.4. MTBF

MTBF, Mean Time between Failures, is a measure of reliability of a device. Its value represents the average time between a repair and the next failure. The unit of MTBF is in hours. The higher the MTBF value, the higher the reliability of the device.

Our MTBF result is based on simulation software (Relex 7.3). Please note that a lower MTBF should be expected for higher capacity drives, and we apply the lowest MTBF for all capacities.

Capacity	MTBF
TLC: 256GB ~ 2TB pSLC: 80GB ~ 640GB	4 million hours

4. ELECTRICAL SPECIFICATIONS



4.1. Supply Voltage

Parameter	Rating
Operating Voltage	3.3V ± 5%
Rise Time (Max/Min)	100ms / 0.1ms
Fall Time (Max/Min)	5s / 1ms
Min. off Time ^{Note1}	1s

Notes:

1. Minimum time between power removed from SSD (Vcc < 100 mV) and power re-applied to the drive.
2. Ensure the voltage of each power domain in SSD has enough time to discharge less than 0.1V.
3. Rise Time during from 10% to 90% of 3.3V.
4. Fall Time during from 90% to 10% of 3.3V.

4.2. Power Consumption

Capacity	Flash Configuration	Standard-Temp.		Wide-Temp.		Idle
		Read	Write	Read	Write	
256GB	256GB x1, BGA(DDP), TLC	2,700	2,400			0.8
512GB	256GB x2, BGA(DDP), TLC	2,800	2,500			0.8
1TB	512GB x2, BGA(QDP), TLC	2,800	2,600			0.8
2TB	1TB x2, BGA(ODP), TLC	2,800	2,600			0.9
80GB	256GB x1, BGA(DDP), pSLC	2,700	2,400	2,700	2,400	0.8
160GB	256GB x2, BGA(DDP), pSLC	2,800	2,500	2,800	2,500	0.8
320GB	512GB x2, BGA(QDP), pSLC	2,900	2,600	2,900	2,600	0.8
640GB	1TB x2, BGA(ODP), pSLC	2,900	2,600	2,900	2,600	0.9

Unit: mW

Notes:

1. Use CrystalDiskMark 8.0.4 with the setting of 1GB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5].
2. The measured power voltage is 3.3V.
3. Idle power consumption is measured at idle state with no write/read operation.
4. It will not enter LPM (Low Power Mode) to avoid complex compatibility issues.
5. Power consumption may differ according to flash configuration, use condition, environment and platform.
6. Measurement environment: Room temperature: 20~25°C, humidity: 40~60%RH, DC+3.3V condition.

5. INTERFACE



5.1. Pin Assignment and Descriptions

The follow table defines the signal assignment of the internal NGFF connector for SSD usage, described in the PCI Express M.2 Specification version 1.1 of the PCI-SIG.

Pin #	PCIe Pin	Description
1	GND	Ground
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	No connect
6	N/C	No connect
7	PETp3	No connect
8	PLN# (I)(0/3.3V)	No connect
9	GND	No connect
10	LED+1# (O)(OD)(3.3V)	These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system. Open drain, active low signal.
11	PERn3	No connect
12	Module Key B	Module Key
13	Module Key B	
14	Module Key B	
15	Module Key B	
16	Module Key B	
17	Module Key B	
18	Module Key B	
19	Module Key B	
20	N/C	No connect
21	GND	Ground
22	VIO 1.8V	No connect
23	PERn2	No connect
24	N/C	No connect
25	PERp2	No connect
26	N/C or GPIO Write Protect	No connect Optional: GPIO Write Protect

Pin #	PCIe Pin	Description
27	GND	Ground
28	N/C	No connect
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	PLA_S3# (O)(0/3.3V)	Power Loss Acknowledge. Open Drain with pull-up on platform.
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	GND	Ground
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	GND	Ground
39	GND	Ground
40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pull-up on platform.
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pull-up on platform.
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	ALERT#(O)(0/1.8V)	Alert notification to master. Open Drain with pull-up on platform. Active low.
45	GND	Ground
46	N/C	No connect
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification. Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	NC	No connect
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only.

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Pin #	PCIe Pin	Description
		Not used in normal operation. Pins should be left N/C in platform Socket.
57	GND	Ground
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67	N/C or GPIO Eease	No Connect Optional: GPIO Erase
68	N/C	No Connect
69	N/C	No Connect for PCIe.
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	VIO_CFG (0)	Sideband IO voltage indication. Signal with a weak pull-up on Platforms that support this function. When the Adapter supports 3.3V on the sideband IO signals, it must be connected to ground on the Adapter, otherwise it must be left unconnected on the Adapter.
74	3.3V	3.3V source
75	GND	CONFIG_2 = Ground

6. SUPPORTED COMMANDS



6.1. NVMe Command List

Table 6-1 Admin Commands

Identifier	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download
14h	Device Self-test
1Dh	NVMe-MI Send
1Eh	NVMe-MI Receive
80h	Format NVM
81h	Security Send
82h	Security Receive
84h	Sanitize

Table 6-2 I/O Commands

Identifier	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
09h	Dataset Management

6.2. Identify Device Command

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 6-3 Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	Serial Number
63:24	M	Model Number (MN)	Model Number
71:64	M	Firmware Revision (FR)	Firmware Name
72	M	Recommended Arbitration Burst (RAB)	0x06
75:73	M	IEEE OUI Identifier (IEEE)	Assigned by IEEE/RAC
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x06
79:78	M	Controller ID (CNTLID)	0x0000
83:80	M	Version (VER)	0x20000
87:84	M	RTD3 Resume Latency (RTD3R)	0x7A120
91:88	M	RTD3 Entry Latency (RTD3E)	0x4C4B40
95:92	M	Optional Asynchronous Events Supported (OAES)	0x200
99:96	M	Controller Attributes (CTRATT)	0x00
101:100	O	Read Recovery Level support bitmap (RRLS)	0x00
110:102	-	Reserved	0x020000000000000000
111	M	Controller Type, if support NVMe 1.4 shall be set to other than 0 (cntrltype)	0x01
127:112	O	FRU Globally Unique Identifier (FGUID[16])	0x00
129:128	O	Command Retry Delay Time 1 (CRDT1)	0x00
131:130	O	Command Retry Delay Time 2 (CRDT2)	0x00
133:132	O	Command Retry Delay Time 3 (CRDT3)	0x00
239:134	-	Reserved	0x00
252:240	O	Reserved for the NVMe Management Interface	0x00
253	O	NVM Subsystem Report (NVMSR)	0x01
254	O	VPD Write Cycle Information (VWCI)	0xFF
255	O	Management Endpoint Capabilities (MEC)	0x3
257:256	M	Optional Admin Command Support (OACS)	0x0057
258	M	Abort Command Limit (ACL)	0x03

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Bytes	O/M	Description	Default Value
259	M	Asynchronous Event Request Limit (AERL)	0x07
260	M	Firmware Updates (FRMW)	0x12
261	M	Log Page Attributes (LPA)	0x3E
262	M	Error Log Page Entries (ELPE)	0xFF
263	M	Number of Power States Support (NPSS)	0x04
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x01
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x016B
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x0170
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x0032
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x4000
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x4000
295:280	O	Total NVM Capacity (TNVMCAP)	By capacity
311:296	O	Unallocated NVM Capacity (UNVMCAP)	0x00
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x00
317:316	O	Extended Device Self-test Time (EDSTT)	0x0A
318	O	Device Self-test Options (DSTO)	0x01
319	M	Firmware Update Granularity (FWUG)	0x01
321:320	M	Keep Alive Support (KAS)	0x0000
323:322	O	Host Controlled Thermal Management Attributes (HCTMA)	0x0001
325:324	O	Minimum Thermal Management Temperature (MNTMT)	0x0111
327:326	O	Maximum Thermal Management Temperature (MXTMT)	0x0166
331:328	O	Sanitize Capabilities (SANICAP)	0xA0000002 (Block Erase) 0xA0000003 (Block Erase & Crypto Erase)
335:332	O	Host Memory Buffer Min. Descriptor Entry Size (HMMINDS)	0x400
337:336	O	Host Memory Maximum Descriptor Entries (HMMAXD)	0x10

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Bytes	O/M	Description	Default Value
339:338	O	NVM Set ID Maximum (NSETIDMAX)	0x00
341:340	O	Endurance Group ID Maximum (ENDGIDMAX)	0x00
342	O	ANA Maximum Transition Time (ANATT)	0x00
343	O	Asymmetric Namespace Access Capabilities (ANACAP)	0x00
347:344	O	ANA Group ID Maximum (ANAGRPMAX)	0x00
351:348	O	Number of ANA Group IDs (NANAGRPID)	0x00
355:352	O	Persistent Event Log Size (PELS)	0x60
257:356	O	Domain Identifier	0x00
367:358	-	Reserved	0x00
383:368	O	Max Endurance Group Capacity (MEGCAP)	0x00
511:384	-	Reserved	0x00
NVM Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	M	Maximum Outstanding Commands (MAXCMD)	0x0100
519:516	M	Number of Namespaces (NN)	0x00000001
521:520	M	Optional NVM Command Support (ONCS)	0x0056
523:522	M	Fused Operation Support (FUSES)	0x0000
524	M	Format NVM Attributes (FNA)	0x04 (OPAL) 0x00 (Pyrite)
525	M	Volatile Write Cache (VWC)	0x07
527:526	M	Atomic Write Unit Normal (AWUN)	0xFF
529:528	M	Atomic Write Unit Power Fail (AWUPF)	0x00
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Namespace Write Protection Capabilities (NWPC)	0x00
533:532	O	Atomic Compare & Write Unit (ACWU)	0x0000
535:534	-	Reserved	0x0000
539:536	O	SGL Support (SGLS)	0x00000000
543:540	O	Maximum Number of Allowed Namespace, if supports ANA Reporting shall not be 0 and less than NN (MNAN)	0x00
559:544	O	Maximum Domain Namespace Attachments (MAXDNA)	0x00
563:560	O	Maximum I/O Controller Namespace Attachments	0x00

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Bytes	O/M	Description	Default Value
767:564	-	Reserved	0x00
IO Command Set Attributes			
1023:768	M	NVM Subsystem NVMe Qualified Name (SUBNQN)	SUBNQN
1791:1024	-	Reserved	0x00
1805:1792	-	Refer to the NVMe over Fabrics specification	0x00
2047:1806	-	Reserved	0x00
2079:2048	M	Power State 0 Descriptor (PSD0)	Bit[15:0] 0x258
2111:2080	O	Power State 1 Descriptor (PSD1)	Bit[124:120] 0x1 Bit[116:112] 0x1 Bit[108:104] 0x1 Bit[100:96] 0x1 Bit[15:0] 0x12C
2143:2112	O	Power State 2 Descriptor (PSD2)	Bit[124:120] 0x2 Bit[116:112] 0x2 Bit[108:104] 0x2 Bit[100:96] 0x2 Bit[15:0] 0x96
2175:2144	O	Power State 3 Descriptor (PSD3)	Bit[124:120] 0x3 Bit[116:112] 0x3 Bit[108:104] 0x3 Bit[100:96] 0x3 Bit[95:64] 0xDAC Bit[63:32] 0x5DC Bit[25] 0x1 Bit[24] 0x1 Bit[15:0] 0x1F4
2207:2176	O	Power State 4 Descriptor (PSD4)	Bit[124:120] 0x4 Bit[116:112] 0x4 Bit[108:104] 0x4 Bit[100:96] 0x4 Bit[95:64] 0xAFC8 Bit[63:32] 0x1388 Bit[25] 0x1 Bit[24] 0x1 Bit[15:0] 0x32

2239:2208	O	Power State 5 Descriptor (PSD5)	0x00
2271:2240	O	Power State 6 Descriptor (PSD6)	0x00
2303:2272	O	Power State 7 Descriptor (PSD7)	0x00
2335:2304	O	Power State 8 Descriptor (PSD8)	0x00
2367:2336	O	Power State 9 Descriptor (PSD9)	0x00
2399:2368	O	Power State 10 Descriptor (PSD10)	0x00
2431:2400	O	Power State 11 Descriptor (PSD11)	0x00
2463:2432	O	Power State 12 Descriptor (PSD12)	0x00
2495:2464	O	Power State 13 Descriptor (PSD13)	0x00
2527:2496	O	Power State 14 Descriptor (PSD14)	0x00
2559:2528	O	Power State 15 Descriptor (PSD15)	0x00
2591:2560	O	Power State 16 Descriptor (PSD16)	0x00
2623:2592	O	Power State 17 Descriptor (PSD17)	0x00
2655:2624	O	Power State 18 Descriptor (PSD18)	0x00
2687:2656	O	Power State 19 Descriptor (PSD19)	0x00
2719:2688	O	Power State 20 Descriptor (PSD20)	0x00
2751:2720	O	Power State 21 Descriptor (PSD21)	0x00
2783:2752	O	Power State 22 Descriptor (PSD22)	0x00
2815:2784	O	Power State 23 Descriptor (PSD23)	0x00
2847:2816	O	Power State 24 Descriptor (PSD24)	0x00
2879:2848	O	Power State 25 Descriptor (PSD25)	0x00
2911:2880	O	Power State 26 Descriptor (PSD26)	0x00
2943:2912	O	Power State 27 Descriptor (PSD27)	0x00
2975:2944	O	Power State 28 Descriptor (PSD28)	0x00
3007:2976	O	Power State 29 Descriptor (PSD29)	0x00
3039:3008	O	Power State 30 Descriptor (PSD30)	0x00
3071:3040	O	Power State 31 Descriptor (PSD31)	0x00
Vendor Specific			
4095:3072	O	Vendor Specific (VS)	Vendor Reserved

Notes:

“O/M”: O = Optional, M = Mandatory.

“-“ : Not support

Table 6-4 Identify Namespace Data Structure & NVM Command Set Specific

Bytes	O/M	Description	Default Value
7:0	M	Namespace Size (NSZE)	-
15:8	M	Namespace Capacity (NCAP)	-
23:16	M	Namespace Utilization (NUSE)	-
24	M	Namespace Features (NSFEAT)	0x00
25	M	Number of LBA Formats (NLBAF)	0x01
26	M	Formatted LBA Size (FLBAS)	0x00
27	M	Metadata Capabilities (MC)	0x00
28	M	End-to-end Data Protection Capabilities (DPC)	0x00
29	M	End-to-end Data Protection Type Settings (DPS)	0x00
30	O	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)	0x00
31	O	Reservation Capabilities (RESCAP)	0x00
32	O	Format Progress Indicator (FPI)	0x00
33	O	Deallocate Logical Block Features (dlfeat)	0x01
35:34	O	Namespace Atomic Write Unit Normal (NAWUN)	0x0000
37:36	O	Namespace Atomic Write Unit Power Fail (NAWUPF)	0x0000
39:38	O	Namespace Atomic Compare & Write Unit (NACWU)	0x0000
41:40	O	Namespace Atomic Boundary Size Normal (NABSN)	0x0000
43:42	O	Namespace Atomic Boundary Offset (NABO)	0x0000
45:44	O	Namespace Atomic Boundary Size Power Fail (NABSPF)	0x0000
47:46	O	Namespace Optimal IO Boundary (NOIOB)	0x0000
63:48	O	NVM Capacity (NVMCAP)	By capacity
65:64	O	Namespace Preferred Write Granularity (NPWG)	0x00
67:66	O	Namespace Preferred Write Alignment (NPWA)	0x00
69:68	O	Namespace Preferred Deallocation(Trim) Granularity (NPDG)	0x00
71:70	O	Namespace Preferred Deallocation(Trim) Alignment (NPDA)	0x00
73:72	O	Namespace Optimal Write Size (NOWS)	0x00
75:74	O	Maximum Single Source Range Length (MSSRL)	0x00
79:76	O	Maximum Copy Length (MCL)	0x00

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Bytes	O/M	Description	Default Value
80	O	Maximum Source Range Count (MSRC)	0x00
91:81	-	Reserved	0x00
95:92	O	ANA Group Identifier (ANAGRPID)	0x00
98:96	-	Reserved	0x00
99	O	Namespace Attributes (NSATTR)	0x00
101:100	O	NVM Set Identifier (NVMSETID)	0x00
103:102	O	Endurance Group Identifier (ENDGID)	0x00
119:104	O	Namespace Globally Unique Identifier (NGUID)	-
127:120	O	IEEE Extended Unique Identifier (EUI64)	-
131:128	M	LBA Format 0 Support (LBAF0)	0x01090000
135:132	O	LBA Format 1 Support (LBAF1)	0x000C0000
383:136	O	LBA Format 2~63 Support (LBAF2~LBAF63)	0x0
4095:384	O	Vendor Specific (VS)	0x00

Notes:

“O/M”: O = Optional, M = Mandatory.

“-”: Not support

■ **List of Identify Namespace Data Structure for Each Capacity**

Capacity (GB)	Byte[7:0]: Namespace Size (NSZE)
256	1DCF32B0h
512	3B9E12B0h
1,024	773BD2B0h
2,048	EE7752B0h
80	950F8B0h
160	12A19EB0h
320	2542EAB0h
640	4A8582B0h

6.3. SMART Attributes

■ SMART Attributes (Log Identifier 02h)

Bytes Index	Bytes	Description	Detail
[0]	1	Critical Warning	Error occurs if value of the bits are not zero
[2:1]	2	Composite Temperature	Flash temperature is detected by thermal sensor (Unit: Kelvin)
[3]	1	Available Spare	Remaining spare capacity available (Unit: %)
[4]	1	Available Spare Threshold	Spare capacity threshold (Unit: %)
[5]	1	Percentage Used	Average of the flash's block erase count / NAND EOL erase count (Unit: %)
[31:6]	26	Reserved	-
[47:32]	16	Data Units Read	(in LBAs) Contains the number of 512byte data units the host has read from the controller. This value is reported in thousands (i.e, a value of 1 corresponds to 1000 units of 512 bytes read) and count up.
[63:48]	16	Data Units Written	(in LBAs) Contains the number of 512byte data units the host has written from the controller. This value is reported in thousands (i.e, a value of 1 corresponds to 1000 units of 512 bytes written) and count up.
[79:64]	16	Host Read Commands	The number of read commands completed by the controller
[95:80]	16	Host Write Commands	The number of write commands completed by the controller
[111:96]	16	Controller Busy Time	The amount of time the controller is busy with I/O commands (Unit: minute)
[127:112]	16	Power Cycles	Normal power on/off cycles count
[143:128]	16	Power On Hours	Device power on time (Unit: hour)
[159:144]	16	Unsafe Shutdowns	Abnormal power on/off cycles count
[175:160]	16	Media and Data Integrity Errors	The number of occurrences where the controller detected an unrecovered data integrity error, such as ECC, CRC checksum failure.
[191:176]	16	Number of Error Information Log Entries	The number of Error Information log entries over the life of the controller.
[195:192]	4	Warning Composite Temperature Time	The amount of time that temp. over warning threshold, but less than critical threshold (Unit: minute)

Bytes Index	Bytes	Description	Detail
[199:196]	4	Critical Composite Temperature Time	The amount of time that temp. over critical threshold (Unit: minute)
[201:200]	2	Temperature Sensor 1 (N/A)	Unit: Kelvin
[203:202]	2	Temperature Sensor 2 (N/A)	Controller junction temperature (Unit: Kelvin)
[205:204]	2	Temperature Sensor 3 (N/A)	Unit: Kelvin
[207:206]	2	Temperature Sensor 4 (N/A)	Unit: Kelvin
[209:208]	2	Temperature Sensor 5 (N/A)	Unit: Kelvin
[211:210]	2	Temperature Sensor 6 (N/A)	Unit: Kelvin
[213:212]	2	Temperature Sensor 7 (N/A)	Unit: Kelvin
[215:214]	2	Temperature Sensor 8 (N/A)	Unit: Kelvin
[219:216]	4	Thermal Management Temperature 1 Transition Count	The number that device enters Thermal Management Temperature 1 (TMT1) Transition Count
[223:220]	4	Thermal Management Temperature 2 Transition Count	The number that device enters Thermal Management Temperature 2 (TMT2) Transition Count
[227:224]	4	Total Time For Thermal Management Temperature 1	The total time in Thermal Management Temperature 1 stage (Unit: second)
[231:228]	4	Total Time For Thermal Management Temperature 2	The total time in Thermal Management Temperature 2 stage (Unit: second)
[511:232]	280	Reserved	

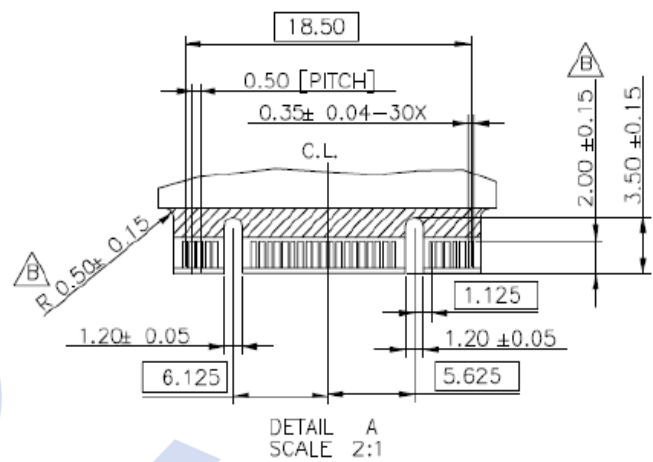
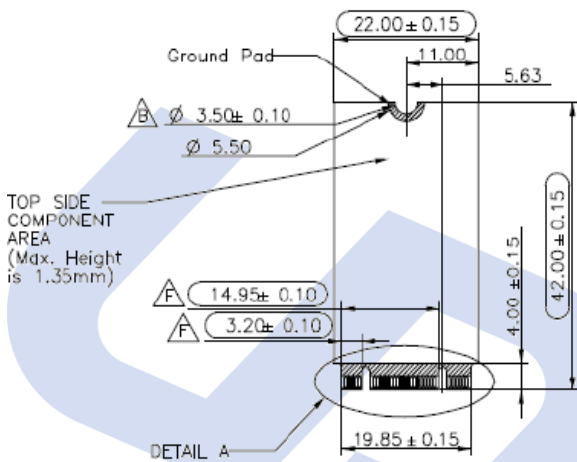
7. PHYSICAL DIMENSION



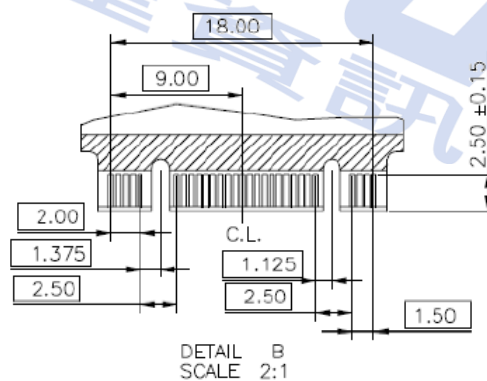
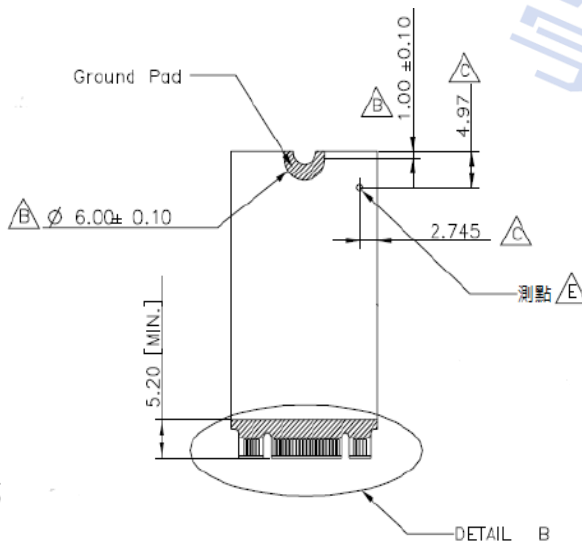
- **Type1: Dimension of M.2 2242-S2-B-M: 42mm(L) x 22mm(W) x 2.15mm(H)**

Top View

Unit : mm



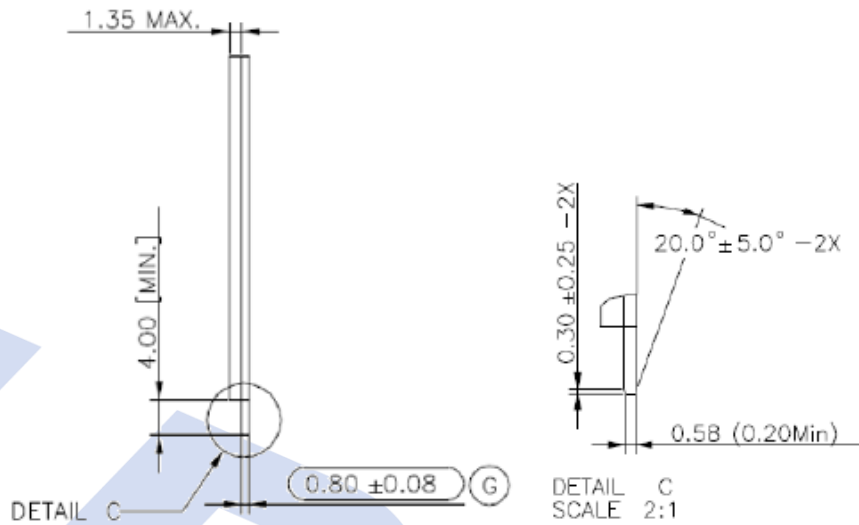
Bottom View



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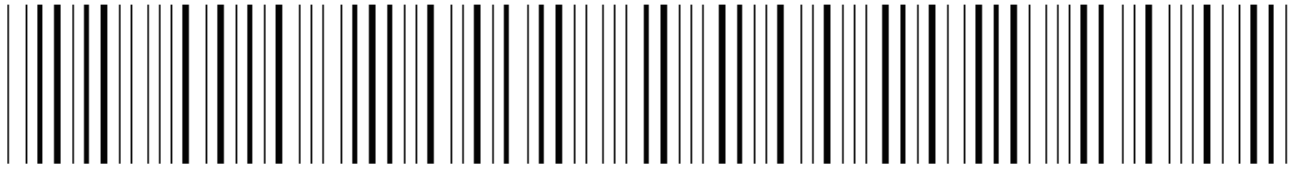
Side View



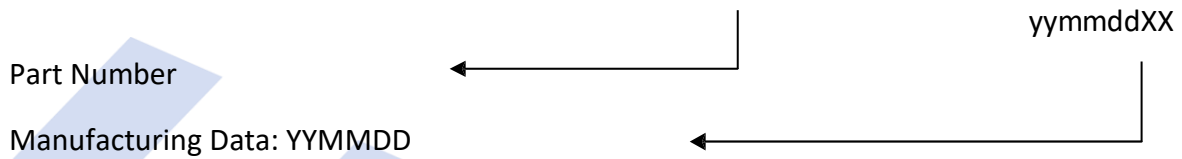
***Notes:**

1. = Max Component Height
2. = No Component
3. = No Component / Signal Vias / Signal Copper / Printing
4. General Tolerance ±0.15mm
5. are critical dimensions

8. BARCODE DESCRIPTION



M 2 P 4 2 D P 0 0 2 T B A G U



9. PART NUMBER DECODER

M2P-42DPX⁸X⁹X¹⁰X¹¹X¹²X¹³X¹⁴X¹⁵X¹⁶X¹⁷

X ¹ X ² X ³	X ⁴ X ⁵	X ⁶ X ⁷	X ⁸ X ⁹ X ¹⁰ X ¹¹ X ¹²	X ¹³	X ¹⁴	X ¹⁵	X ¹⁶ X ¹⁷
M2P	42	DP	256GB 512GB 001TB 002TB	080GB 160GB 320GB 640GB A: 3D TLC Standard (0°C ~ +70°C) V: 3D pSLC Standard (0°C ~ +70°C) W: 3D pSLC Industrial (-40°C ~ +85°C)	G	U	blank